REMARKS

Claim 1 has been amended in the application. New claims 2-24 have been added. Accordingly, claims 1-24 are currently pending in the application.

In the Office Action, the Examiner objected to the Abstract of the disclosure because it should be 150 words or less; and rejected claim 1 under 35 USC § 102(b) as being anticipated by U.S. Patent No. 4,573,023 to Cok et al.

By this Amendment, the Abstract has been amended to overcome the objection; and claim 1 has been amended. Additionally, Applicants now present new claims 2-24.

The prior art rejection is traversed. Arguments in support thereof are provided.

It is further respectfully submitted that the within amendments introduce no new matter within the meaning of 35 U.S.C. §132.

Objection to the Abstract

The Examiner objected to the Abstract as being too lengthy. In response, Applicants have amended the Abstract to be 150 words or less.

As the Abstract now complies with MPEP 608.01(b), Applicants respectfully request that the objection be withdrawn.

Rejection under 35 USC § 102(b)

The Examiner rejected claim 1 as being anticipated by Cok et al.

Reconsideration and withdrawal of the rejection is respectfully requested.

The test for anticipation under section 102 is whether each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053

(Fed. Cir. 1987); MPEP §2131. The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989); MPEP §2131. The elements must also be arranged as required by the claim. *In re Bond*, 15 USPQ2d 1566 (Fed. Cir. 1990).

It is respectfully submitted that Cok et al. fails to disclose each and every element as set forth in independent claim 1.

Claim 1 has been amended by associating a value "*Fref*" with the reference voltage, "*Fosc*" with the desired frequency, and "*P/Q*" with the expression of their ratio *Fosc/Fref*. As discussed on page 19, paragraph beginning on line 3 in the specification of this application, a frequency *Fosc* and a frequency *Fref* always have a rational relationship which can be represented as a ratio of two integer numbers *P* and *Q*.

The inventive subject matter of the present invention is defined in the ratio *P/Q* further expanded as shown in equation (7) on page 20, line 25 of the specification: $Fosc/Fref = P/Q = \pm 1/p_1 \pm 1/p_2 \pm \ldots 1/p_n$, and where it can be realized in hardware specifically as discussed on page 19, paragraph beginning on line 27 and continuing to page 20 line 26 of the specification, namely using SSB mixing for addition and subtraction of the terms, and frequency division for realizing the fractional terms.

In contrast, Cok et al. discloses a multiple-multiple modulus prescaler for a phase-locked loop (PLL). The device in Cok et al. essentially consists of a PLL having a multiple modulus divider in the VCO 18 path, optionally accompanied by a frequency offset achieved by means of an SSB mixer 22 in the VCO 18 path. It appears that the programmable frequency divider 34 is constructed using common digital logic building

blocks for example, dividers 52, programmable counters 40, and rate multipliers 46, to achieve a frequency translation.

Although both Cok et al. and the instant invention may have the same goal of devising a PLL synthesizer able to be tuned in small fractional steps, the methods employed are significantly different. Claim 1 is different from Cok et al. for the following reasons:

a) the frequency translation method disclosed in Cok et al. does not rely on the combination of dividers and SSB mixers to implement a mathematical fraction expression as recited in claim 1, but rather relies on a different concept for achieving frequency fractions, namely programmable counters in conjunction with multiple-modulus dividers, and rate multipliers (*cf.* Figures 2 and 3 of the present invention with Figure 1 of Cok et al.);

b) the PLL synthesizer disclosed and recited for example, in the independent claims has a frequency translation performed in the reference path (see Figures 2 and 3 of the instant invention), while the frequency translation mechanism disclosed in Cok et al. (which might also include an SSB mixer) is in the VCO path of the PLL (*cf.* with Figure 1 of Cok et al.); i.e., in the present invention the frequency translation is applied directly on the reference signal and then the result is compared with the VCO output reference frequency directly, thus maintaining the highest possible comparison frequency (not divided), and therefore achieving

superior phase noise (see paragraph beginning on line 16 of page 7 of the specification of the instant application); while on the other hand, the VCO 18 in Cok et al. is offset by SSB mixer 22 and translated by divider 34 prior to the phase comparison at the phase detector 14;

c) the frequency translation method and apparatus as disclosed and claimed do not involve any multiple-modulus dividers or rate multipliers, while in Cok et al. they constitute essential elements.

To summarize, Cok et al. fails to teach or suggest each and every limitation of claim 1, namely, a frequency ratio generator coupled to a phase detector, for generating a desired frequency *Fosc* based on a fraction expansion of a ratio *P/Q* of the desired frequency *Fosc* and the reference frequency *Fref*, whereby all additions are realized by an upper side-band SSB mixer, all subtractions are realized by a lower-side-band SSB mixer and all fractions are realized by frequency dividers.

Thus, it is therefore respectfully submitted the claimed method and apparatus are materially different from the cited reference. Accordingly, as the Cok et al. patent does not teach or suggest all of the claim limitations of the present invention; Applicants respectfully submit that claim 1 as amended patentably distinguishes over Cok et al. taken alone or in combination.

Therefore, Applicants request that the rejection of independent claim 1 under 35 USC § 102(b) be withdrawn.

Further, new claims 2-24 should be allowed for at least similar reasons discussed in detail above with reference to claim 1. Specifically, Applicants submit that claims 2-9 are allowable as being dependent on claim 1.

Particularly, new independent claim 10 and its dependent claims are allowable at least for the same reasons as discussed regarding claim 1 since it recites a methodology for synthesizing the PLL device of claim 1, which comprises a novel Frequency Ratio Generator (FRG) method of translation.

New independent claim 19 and its dependent claim are allowable at least for the reason that it recites a combination of features, *inter alia*, producing an FRG output signal directly (without a PLL) having a dominant frequency $Fg = P/Q \cdot Fin$, expressed in a fraction expansion form, realizing all additions by upper side-band SSB mixing, all subtractions by lower-side-band SSB mixing and all the fractions by frequency division. Support for claim 19 can be found for example on pages 20 - 21 of the specification and Figures 2 and 3.

New independent claim 21 and its dependent claim are allowable at least for the same reasons as claim 19, since it recites a methodology for translating the FRG device of claim 19 to produce an output signal directly (without a PLL) having a dominant frequency $Fg = P/Q \cdot Fin$.

New independent claim 23 is allowable at least for the reason that it recites a combination of features, *inter alia*, a PLL comprising a novel FRG translating device coupled in a slightly different way than recited in claims 1 and 10. In this case while $Fg = R/S \cdot Fo$ the output frequency $Fo = S/R \cdot Fref$. Support for claim 23 can be found for

example in equation *6a* on page 19 of the specification (the case where in *6a* P1 corresponds to R, Q1 to S and P2/Q2 ratio is equal 1).

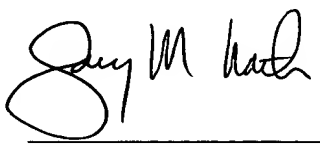
New independent claim 24 is allowable at least for the reason that it recites a methodology for synthesizing a PLL as expressed in claim 23, comprising a novel FRG method of translation coupled in a slightly different way than recited in claims 1 and 10. In this case while $Fg = R/S \cdot Fo$ the output frequency $Fo = S/R \cdot Fref$. Support for claim 6 can be found for example in equation *6a* on page 19 of the specification (case where in *6a* P1 corresponds to R, Q1 to S and P2/Q2 ratio is equal 1).

CONCLUSION

In light of the foregoing, Applicants submit that the application is now in condition for allowance. If the Examiner believes the application is not in condition for allowance, Applicants respectfully request that the Examiner contact the undersigned attorney if it is believed that such contact will expedite the prosecution of the application. Favorable action with an early allowance of the claims is earnestly solicited.

Respectfully submitted,

NATH & ASSOCIATES PLLC



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Gary M. Nath
Reg. No. 26,965
Gregory B. Kang
Reg. No. 45,273
Teresa M. Arroyo
Reg. No. 50,015
Customer No. 20529

NATH & ASSOCIATES PLLC
1030 15th Street, N.W.
6th Floor
Washington, D.C. 20005
Tel: (202) 775-8383
Fax: (202) 775-8396